

VIDEO CAMERA IMAGER AND IMAGER IC CAPABLE OF
PLURAL KINDS OF DOUBLE-IMAGE PROCESSINGS

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The invention generally relates to an imaging method and apparatus for use in a video camera and more specifically to an imager that can operate in one of at least two double-image processing modes.

2. Description of the Prior Art

10 Conventional television systems such as the NTSC (National Television System Committee) system are using the interlace scanning. However, the sequential scanning has come to be used for a higher resolution. Also, in order to widen the dynamic range of an imaging apparatus, some of the imagers adopt a dynamic range-widening scan scheme by using a CCD device having twice the number of pixels in the vertical direction.

15 Since ICs (integrated circuits) are increasing in the scale, developing an imager IC (integrated circuit) dedicated to one of above-mentioned applications in response to a specific demand would result in a late release of a desired article.

20 However, if an imager were simply arranged to meet each of the above applications, the circuit scale of the imager would become too large.

 Accordingly, it is an object of the invention to provide an imaging method and apparatus that efficiently support the interlace scan mode, the dynamic range-widening scan mode and the sequential scan mode with a limited amount of circuitry.

25 It is another object of the invention to provide an imager IC that efficiently supports the interlace scan mode, the dynamic range-widening scan mode and the sequential scan mode with a limited amount of circuitry.

SUMMARY OF THE INVENTION

According to the invention, an imager, for use in a video camera, which can operate in any of an interlace scan mode, a dynamic range-widening scan (WS) mode and a sequential scan mode. The imager comprises
5 a CCD portion, responsive to a mode selection signal, for generating a corresponding one of an interlace scan image signal, a WS image signal of $2N$ lines and a sequential scan image signal of $2N$ lines (N is the number of scan lines of an image to be obtained). Every other line of WS image signal is longer in exposure time than adjacent lines of the WS image signal. Each pair
10 of odd lines and even lines of the WS image signal and the sequential scan image signal is synchronized by two $1H$ -memories. In the WS mode, a synchronized pair of odd and even lines of the WS image signal is added together by a mixer to become a dynamic range-widened image signal. The interlace scan image signal, the dynamic range-widened image signal and a
15 pair of odd line signal and even line signal of the sequential scan image signal are subjected to the image signal regulation by a image signal regulator.

In the interlace scan mode, the regulated interlace scan image signal is output through a first input of an alternative selector. In the WS mode, the regulated dynamic range-widened image signal is output through the first
20 input of the alternative selector. In the sequential scan mode, the regulated odd line signal and even line signal of the sequential scan image signal are combined by a sequential scan image signal generator into a new sequential scan image signal for output. Also, in the sequential scan mode, the odd line signal and the even line signal of the sequential scan image signal are added
25 together by an adder to become a new image signal equivalent to the interlace scan image signal, which new image signal is output through the second input of the alternative selector.

In one embodiment, a simplified imager supports only the interlace scan mode and the sequential scan mode.

In another embodiment, a simplified imager supports only the WS mode and the sequential scan mode.

5 In the IS and WS modes, the image signal regulator calculates a vertical contour correction value for the current line from 5 lines centered on the current line. In the SS mode, the image signal regulator calculates a vertical contour correction value for each of the current odd line and even line from 6 lines centered on two current odd and even lines.

10 BRIEF DESCRIPTION OF THE DRAWING

Further objects and advantages of the present invention will be apparent from the following description of the preferred embodiments of the invention as illustrated in the accompanying drawing, in which:

FIG. 1 is a block diagram showing an exemplary arrangement of an imager that effectively supports interlace scan (IS) operation, dynamic range widening scan (WS) operation and sequential scan (SS) operation in accordance with an illustrative embodiment of the invention;

FIG. 2 is a diagram showing output image signals a CCD portion 14 of FIG. 1 provides in IS, WS and SS operations;

20 FIG. 3 is a table useful in understanding the operation of the imager 1 of FIG. 1;

FIG. 4 is a block diagram showing an exemplary structure of an image signal regulator 50 of FIG. 1;

FIG. 5 is a block diagram showing an exemplary arrangement of an imager that effectively supports IS and SS operations in accordance with a modification of the embodiment of FIG. 1; and

FIG. 6 is a block diagram showing an exemplary arrangement of an

imager that effectively supports WS (dynamic range widening scan) and SS operations in accordance with another modification of the embodiment of FIG. 1.

Throughout the drawing, the same elements when shown in more than one figure are designated by the same reference numerals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic functional block diagram showing an exemplary arrangement of an imager 1 that effectively supports interlace scan (IS) operation, dynamic range widening scan (WS) operation and sequential scan (SS) operation in accordance with an illustrative embodiment of the invention. In FIG. 1, the imager 1 comprises an optical and mechanical portion (OMP) 10 for focusing into an image of the object to be shot; an OMP driver 12 for driving the optical and mechanical portion 10 in responsive to control signals supplied from the external; a CCD (charge coupled device) portion 14 that operates in one of three (i.e., IS, WS and SS) operation modes in response to a IS/WS/SS selection signal supplied from the outside of the imager 1 (i.e., from a not-shown controller for controlling the entire video camera in which the imager 1 is used); a preprocessor 16 for effecting analog processing (e.g., AGC (automatic gain control)) of the image signal from the CCD portion 14; an analog-to-digital converter (A/C) 18 for converting the analog image signal from the preprocessor 16 into a digital image signal; a synchronizer 30 for providing a time axis conversion in the dynamic range widening scan (WS) operation or in the sequential scan operation; a signal mixer 40 for mixing two image signals of different exposure (or charging) times into a dynamic range-widened image signal in the WS operation mode; an image signal regulator 50 for providing basic

camera signal processing such as contour correction; a sequentially scanned image signal generator 60 for composing a single sequential scan image signal from an odd line field signal and an even line field signal into which a sequential scan image signal has been separated by the time axis conversion
5 30 in the SS mode; an IS and WS signal output portion 70 for outputting an IS or WS image signal depending on the operation mode; and an imager controller 80 for supplying various control signals to respective elements as detailed later.

Specifically, the synchronizer 30 comprises a first alternative selector
10 32 having one data input 32A connected to the A/D 16 output and its control input terminal connected to an output C1 terminal of the imager controller 80; two 1-line memories (1H) 34 which each store a horizontal line's worth of pixel data and which have their input ports connected together to the selector 32 common terminal; and a second alternative selector 36 having one data
15 input 36A connected to the A/D 16 output (and accordingly to the selector 32 input 32A), the other data input 36B connected to a first one (e.g., 34-1) of two 1H-memories 34 and its control input terminal connected to an output C2 terminal of the imager controller 80.

The signal mixer 40 comprises a mixer 42 having its one data input
20 42L connected to the selector 36 common terminal, its the other data input 42S connected to a second one (34-2 in this specific example) of two 1H-memories 34 and its control input connected to a control output WS of the imager controller 80; and a third alternative selector 44 having one data input
25 44A connected to the selector 36 common terminal and the mixer input 42L, the other data input 44B connected to the mixer 42 output and a selector 32 input 32B and its control input terminal connected to the control output WS of the imager controller 80. The control signal WS takes a binary value

depending on whether the operation mode of the imager 1 (or the CCD
portion 14) is in the dynamic range widening scan (WS) mode or not. It is
assumed that the signal WS is logical "1" in case of the WS mode. Then, the
mixer 42 is so arranged as to add the L input signal, which has been longer
5 exposed or charged, and the S input signal, which has been shorter exposed or
charged, yielding a dynamic range-widened image signal and to effect an
gradation correction on the dynamic range-widened image signal if the
imager 1 is in the WS mode. Though the common terminal of the alternative
selector 36 is supplied to the A input of selector 44 in the interlace scan (IS)
10 mode and the sequential scan (SS) mode, the selector 36 common terminal
may be gradation corrected in the mixer 42 and then supplied to the B input of
the selector 44 in the IS and SS modes.

The image signal regulator 50 has one data input connected a
common terminal of the alternative selector 44, the other data input connected
15 to the second IH memory 34-2 and the mixer input 42S, and its control input
connected to a control output SS of the imager controller 80. The image
signal regulator 50 is detailed later.

The IS and WS (or Sm) signal output portion 70 comprises an adder
72 that is utilized in the SS mode for adding the first and second outputs of
20 the image signal regulator 50, which are an odd line signal and an even line
signal in the mode, to generate an interlace scanned image signal; and a third
alternative selector 74. The image signal regulator 50 first output is connected
to an (odd) input of the SS image signal generator 60, the adder 72 first input
and a first input of the adder 72 and a selector input 74B. The image signal
25 regulator 50 second output is connected to an (even) input of the SS image
signal generator 60 and the adder 72 second input. The selector 74 has its
control input connected to the SS control output of the imager controller 80.

1 The SS control signal takes a binary value depending on whether the imager 1
or the CCD portion 14 is in the SS mode or not. The selector 74 and the
controller 80 (or the control signal SS) is so configured as to output the
selector 74A input signal in the SS mode and to output the selector 74B input
5 signal in other scan or operation mode.

FIG. 2 is a diagram showing output image signals a CCD portion 14
of FIG. 1 provides in response to a Cccd control signal from the controller 80.
The Cccd control signal takes three values corresponding to the IS, WS and
SS operation modes. As shown in FIG. 2, the CCD portion 14 outputs an IS
10 image signal S_i in the IS mode: i.e., outputs an image or field signal of $N/2$
odd lines and an image signal of $N/2$ even lines successfully every $1/30$
seconds. The number N is the number of horizontal scanning lines of an
image to be obtained. In the dynamic range widening scan (WS) mode, the
CCD portion 14 outputs an image of $2N$ lines every second one of which
15 differs in the exposure (or charging) time from the adjacent lines every $1/30$
seconds. And, in the sequential scan (SS) mode, the CCD portion 14 outputs
an image of $2N$ horizontal scan lines every $1/30$ seconds.

FIG. 3 is a table useful in understanding the operation of the imager 1
of FIG. 1. In the table, a symbol "X" indicates that a corresponding element is
20 not used or disabled in the mode. Symbols "A" and "B" in the selector
columns indicate that the selector outputs the signal applied to the input
terminal labeled with the specified symbol.

Referring to FIGS. 1 through 3, the operation of the imager 1 is
described in the following.

25 Interlace Scan Mode

If a mode specifying command or signal (IS/WS/SS selection signal)
from the not-shown controller of the camera in which the imager 1 is used

indicates the IS mode, then the above-mentioned IS image signal S_i is output from the A/D 16. In this case, the control signal C1 disables the selector 32 and control signal C2 causes the selector 36 to select the A input signal or output the signal S_i , which is basically applied to the selector 44 input A.

- 5 Since the input 44A is selected, the signal S_i is input to the linked input of image signal regulator 50 to be subjected to a contour correction and appears at the corresponding regulator 50 output. Since the B input is coupled to the common terminal in the selector 74, the contour-corrected IS image signal S_i is output from the selector 74 common terminal.

- 10 In the above example, the signal S_i is passed, as it is, to the image signal adjustor 50 by controlling the selector 44 to select its A input. However, the mixer 42 and the selector 44 may be arranged such that the mixer 42 executes only a gradation correction and the selector 44 selects its B input.

Dynamic Range-Widening Scan Mode

- 15 If the mode specifying command or IS/WS/SS selection signal indicates the IS mode, then the above-mentioned WS image signal S_w is output from the A/D 16. Since the selector 32 selects its A input as shown in FIG. 3, the selector 32 outputs the signal S_w . Each of the long exposed lines ($\{H(2n-1) | n = 1, 2, \dots, N\}$ in the specific example of FIG. 2) is stored in the
- 20 1H-memory 34-1, while each of the shortly exposed lines ($\{H(2n) | n = 1, 2, \dots, N\}$ in the specific example of FIG. 2) is stored in the 1H-memory 34-2. The long exposed line data $H(2n-1)$ and the shortly exposed line data $H(2n)$ stored in the 1H-memories 34 are simultaneously read out and supplied to the mixer 42 respective inputs L and S through the selector 36 input B and
- 25 common terminal. The mixer 42 calculates the sums of corresponding pixels of the long $H(2n-1)$ and shortly $H(2n)$ exposed lines which sums constitute a dynamic range-widened image signal S_m and gradation corrects the image

signal S_m , which is supplied to the image signal regulator 50 through the selector 44 input B and common terminal. The regulated image signal S_m is output through the selector 74 input B and common terminal.

Sequential Scan Mode

5 If the mode specifying command or IS/WS/SS selection signal indicates the SS mode, then the above-mentioned SS image signal S_s is output from the A/D 16. Since the selector 32 selects its B input and the selector 36 selects its A input as shown in FIG. 3, the signal S_s is supplied to the mixer 42 input L through selector 36 input A. In this case, the mixer 42 is so
10 arranged as to effect only a gradation correction on the L input signal or signal S_s . Since the selector 44 is selecting its A input and the selector 32 is selecting B, the gradation-corrected signal S_s appears at the selector 32 common terminal. Each odd line and each even line of the signal S_s are stored in the 1H-memories 34-1 and 34-2, respectively. The odd line data $H(2n-1)$
15 and the even line data $H(2n)$ stored in the 1H-memories 34 are simultaneously read out and supplied to the image signal regulator 50 through the selector 44 input A and common terminal. This is because the mixer 42 is so arranged as to become in active just after the gradation correction of signal S_s . The odd and even line signals are regulated by the image signal regulator 50.

20 The regulated odd and even line signals are combined into a sequentially scanned image signal in the SS image generator 60 and output as the SS image signal. Also, the regulated odd and even line signals are added together by the adder 72 to become an image signal equivalent to the interlace scanned image signal. Thus obtained interlace scan image signal is output
25 through the selector 74 input A and common terminal. Thus, if the CCD portion 14 or the imager 1 is operated in the SS mode, the imager 1 can provide not only an SS image signal from the SS image generator 60 but also

an IS image signal from the selector 74 common terminal.

As described above, the inventive imager 1 can effectively support the interlace scan operation, the dynamic range widening scan operation and the sequential scan operation.

5 FIG. 4 is a block diagram showing an exemplary structure of an image signal regulator 50 of FIG. 1. In FIG. 4, the image signal regulator 50 comprises a first 1H-memory 52 having its input connected to the Si/Sm/odd input terminal thereof; a second 1H-memory 53 having its input connected to the 1H-memory 52 output; a selector 51 having its input A connected to the 10 1H-memory 53 output; a third 1H-memory 54 having its input connected to the selector 51 common terminal; a fourth 1H-memory 55 having its input connected to the 1H-memory 54; a vertical contour correction portion 56 having its 6 inputs connected to all the input and output ports of the first through fourth 1H-memories 52 through 55; an alternative selector 57; and a 15 current line signal processor 58. The A input of the selector serves as a current odd line input terminal and is connected with the node among 1H-memories 52 and 53 and the linked input of the element 56. The B input of selector 57 serves as a current line input terminal for Si or Sm image signal and is connected with the node among the 1H-memory 53 output, selector 51 20 input A and the linked input of element 56. The control input terminals of selectors 51 and 57 are connected to the SS control output terminal of the imager controller 80. The selector 57 common terminal is connected to a first input terminal of the current line signal processor 58. The second input terminal of the processor 58 is connected with the node among the 1H- 25 memories 54 and 55 and the linked input terminal of element 56. The element 56 output is supplied to the current line signal processor 58. The output terminals of the processor 58 serves as the output terminals of the image

signal regulator 50.

In the IS and WS modes, assuming the current horizontal line to be expressed as $H(i-2)$, lines $H(i-4)$ through $H(i)$ of image data are supplied to the input terminals of the vertical contour correction portion 56. In other words, the vertical contour correction value for the current line $H(i-2)$ is calculated from 5 lines $H(i-4)$ to $H(i)$.

In the SS mode, assuming the current odd and even horizontal lines to be expressed as $H(2i-3)$ and $H(2i-2)$, respectively, lines $H(2i-5)$ through $H(2i)$ of image data are supplied to the input terminals of the vertical contour correction portion 56. In other words, the vertical contour correction values for the current odd $H(2i-3)$ and even $H(2i-2)$ lines are calculated from 6 lines $H(2i-5)$ to $H(2i)$.

The arrangement of the inventive image signal regulator 50 enables a highly accurate vertical contour correction with a limited scale of circuit.

15 Modifications

FIG. 5 is a block diagram showing an exemplary arrangement of an imager 1a that effectively supports IS and SS operations in accordance with a modification of the embodiment of FIG. 1. In FIG. 5, the imager 1a is identical to that of FIG. 1 except that the CCD portion, the synchronizer and the imager controller have been changed from 14, 30 and 80 to 14a, 30a and 80a, respectively; and the mixer 40 has been eliminated. The CCD portion 14a has only the IS and SS modes. The selector 32 has been eliminated and the A/D 16 output is directly supplied to the 1H-memories 34.

In the IS mode, a regulated IS signal S_i is output from the selector 74 output. In the SS mode, the SS image signal generator 60 outputs a regulated SS image signal while the selector 74 outputs the regulated IS image signal.

FIG. 6 is a block diagram showing an exemplary arrangement of an

imager 1b that effectively supports WS (dynamic range widening scan) and SS operations in accordance with another modification of the embodiment of FIG. 1. . In FIG. 6, the imager 1b is identical to that of FIG. 1 except that the CCD portion and the synchronizer and the imager controller have been
5 changed from 14, 30 and 80 to 14b, 30b and 80b, respectively. The CCD portion 14b has only the WS and SS modes. The selectors 32 and 36 have been eliminated and the A/D 16 output is directly supplied to the 1H-memories 34.

In the WS mode, a regulated and dynamic range-widened image
10 signal is output from the selector 74 common terminal. In the SS mode, the SS image signal generator 60 outputs a regulated SS image signal while the selector 74 outputs the regulated IS image signal.

It should be noted that the above-described circuits has been implemented by using discrete components. However, each of the circuit 30
15 through 80 in FIG. 1, the circuit 30a through 80a of FIG. 5 and the circuit 30b through 80b of FIG. 6 may be implemented as an integrated circuit (IC) or a part of any IC.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present
20 invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.